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PATENT APPLICATION

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IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Gerald L. EVERETT et al.

Confirmation No.: 5509

Application No.: 10/737,106

Examiner: Choi, W. H.

Filing Date: 12/15/03

Group Art Unit: 2189

Title: A PLATFORM INDEPENDENT METHOD FOR ESTABLISHING A RUN-TIME DATA AREA

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TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on 01/18/07.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☐ 1st Month $120	☐ 2nd Month $450	☐ 3rd Month $1020	☐ 4th Month $1590

☐ The extension fee has already been filed in this application.

☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 500. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Respectfully submitted,

Gerald L. EVERETT et al.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellant:	Everett et al.	Patent Application	
Serial No.:	10/737,106	Group Art Unit:	2189
Filed:	12/15/2003	Examiner:	Choi, Woo

For: A Platform Independent Method For Establishing A Run-Time Data Area

Appeal Brief

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Real Party in Interest

The assignee of the present invention is Hewlett-Packard Company.

Related Appeals and Interferences

There are no related appeals or interferences known to the Appellant.

Status of Claims

Claims 1-24 stand rejected. Rejections of claims 1-24 are herein appealed.

Status of Amendments

All proposed amendments have been entered. An amendment subsequent to the Final Action has not been filed.

Summary of Claimed Subject Matter

A computer implemented method 300 (Figure 3 and pages 12-13) for establishing a run-time data area is disclosed. The method 300 includes relocating 310 a firmware module (210 of Figures 2A and 2B) from a read-only memory (604 of Figure 2) location to a writeable memory location (603 of Figure 2A) during a system boot-up operation. The method further includes reserving 320 a portion of the writeable memory location comprising a memory allocation for the firmware module (210 of Figure 2) and an additional memory allocation. The method also includes designating 330 the additional memory allocation as the run-time data area, wherein the run-time data area is created without requiring prior knowledge of system resource allocation.

A method 400 (Figure 4 and page 13) for creating a system independent run-time data storage area is also disclosed. The method 400 includes intercepting 410 a system call for determining the size of a system firmware feature (210 of Figures 2A and 2B) during a system boot-up operation. The method 400 also includes returning 420 a response to the system call conveying a request for a portion of a writeable memory location (603 of Figure 2B). Method 400 also includes reserving 430 a portion of the writeable memory location, wherein a memory allocation is designated as the run-time data area (213 of Figure 2B), wherein the run-time data area is created without requiring prior knowledge of system resource allocation.

Grounds of Rejection to be Reviewed on Appeal

1. Claims 2-4 and 13 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention.

2. Claims 1-3, 8-14 and 18-22 stand rejected under 35 U.S.C. 102(e) as being anticipated by Cepulis (U.S. Patent Application Publication No. 2004/0123092).

3. Claims 1, 8 and 18 stand rejected under U.S.C. 102(e) as being anticipated by Malek (U.S. Patent No. 6,611,912).

4. Claims 5-7, 15-17 and 23-25 under 35 U.S.C. 103(a) as being unpatentable over Malek in view of Fish (U.S. Patent No. 6,199,159).

Arguments

1. Whether Claims 2-4 and 13 are indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention.

Claims 2-4 and are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. Applicants submit that the rejection of Claims 2-4 under 35 U.S.C 112, second paragraph is improper because there is sufficient antecedent basis for the limitation "said system call requesting said memory allocation."

In the response to arguments portion of the Office Action mailed 10/18/2006, the Examiner states that the limitation "receiving a system call for a system firmware feature" is not antecedent basis for "returning a response to said system call requesting said memory allocation" because there is no recitation of "a system call requesting" any memory allocation prior to the limitation in question. Applicants respectfully assert that this rejection is improper because the Applicants have fulfilled the requirements for providing antecedent basis for the limitation in question.

2. Whether Claims 1-3, 8-14 and 18-22 are anticipated by Cepulis (U.S. Patent Application Publication No. 2004/0123092).

REJECTION DOES NOT SATISFY REQUIREMENTS OF A *PRIMA FACIE* CASE OF ANTICIPATION

According to the Federal Circuit, "[a]nticipation requires the disclosure in a single prior art reference of each claim under consideration" (W.L. Gore & Assocs. v. Garlock Inc., 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983); see also MPEP 2131). However, it is not sufficient that the reference recite all the claimed elements. As stated by the Federal Circuit, the prior art reference must disclose each element of the claimed invention "arranged as in the claim" (emphasis added; Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984); see also In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990); see also MPEP 2131). In other words "[t]he identical invention must be shown in as complete detail as is contained in the ...claim" (emphasis added; Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); see also MPEP 2131).

KEY CLAIM LIMITATIONS THAT ARE NOT MET BY THE CITED ART

Claim 1 sets forth a computer implemented method for establishing a run-time data area comprising:

relocating a firmware module from a read-only memory location to a writeable memory location during a system boot-up operation;

reserving a portion of said writeable memory location comprising a memory allocation for said firmware module and an additional memory allocation; and

designating said additional memory allocation as said run-time data area, wherein said run-time data area is created without requiring prior knowledge of system resource allocation.

In the current Office Action mailed 10/18/2006, the Examiner makes reference to Cepulis supporting the grounds of rejection. However, Applicants do not understand Cepulis to teach or suggest "relocating a firmware module from a read-only memory location to a writeable memory location during a system boot-up operation," as claimed in Independent Claim 1. Independent Claims 8 and 18 recite similar limitations. In paragraph 17, Cepulis teaches "the computer system may have the capability of logically partitioning the computer resources and then executing multiple operating systems, one in each partition." This is very different from "relocating a firmware module from a read-only memory location to a writeable memory location during a system boot-up operation," as claimed.

For this rational, Cepulis does not teach each and every element of Independent Claims 1, 8 and 18. Therefore, the rejection of Claim 1-4, 8-14 and 18-22 under 35 U.S.C. 102(e) as being anticipated by Cepulis is improper and should be reversed.

3. Whether Claims 1, 8 and 18 are anticipated by Malek (U.S. Patent No. 6,611,912).

In the Office Action mailed 10/18/2006, the Examiner makes reference to Malek supporting the grounds of rejection. However, Applicants do not understand Malek to teach or suggest "relocating a firmware module from a read-only memory location to a writeable memory location during a system boot-up operation," as claimed. Malek purports to teach in column 2, lines 33-40 "the present invention provides a process and means for enumeration of multiple devices/functions on a riser card.....This is accomplished by creating a virtual add-on ROM that the BIOS will detect naturally."

Malek further teaches in 404 of Figure 4 "ROM contents are shadowed into main memory." Shadowing contents is very different from "relocating a firmware module from a read-only memory location to a writeable memory location during a system boot-up operation," as claimed. With the present invention, the firmware is relocated and not shadowed, as with Malek. For this rational, the rejection of Claims 1, 8 and 18 under U.S.C. 102(e) as being anticipated by Malek is improper and should be reversed.

4. Whether Claims 5-7, 15-17 and 23-25 are unpatentable over Malek in view of Fish (U.S. Patent No. 6,199,159).

The rejection of Claims 5-7, 15-17 and 23-25 under U.S.C. 103(a) as being unpatentable over Malek in view of Fish is improper because key claim limitations are not met by the cited references. Specifically, neither Malek nor Fish teach or suggest "relocating a firmware module from a read-only memory location to a writeable memory location during a system boot-up operation," as claimed.

As stated above, Malek to teach or suggest "relocating a firmware module from a read-only memory location to a writeable memory location during a system boot-up operation," as claimed. Furthermore, Fish fails to teach or suggest "relocating a firmware module from a read-only memory location to a writeable memory location during a system boot-up operation," as claimed. For this rational, the rejection of Claims 5-7, 15-17 and 23-25 as being unpatentable over Malek in view of Fish is improper and should be reversed.

In summary, the Appellant respectfully requests that the Board reverse the Examiner's rejections of claims 1-30. Specifically, Applicants respectfully submit that the Examiner's rejections of the Claims are improper as the rejection of Claims 1-3, 8-14 and 18-22 under 35 U.S.C. 102(e) as being anticipated by Cepulis does not satisfy the requirements of a prima facie case of anticipation as claim limitations are not met by the cited reference.

Moreover, Applicants respectfully submit that the Examiner's rejection of the Claims is improper as the rejection of Claims 1, 8 and 18 under U.S.C. 102(e) as being anticipated by Malek does not satisfy the requirements of a prima facie case of obviousness as claim limitations are not met by the cited reference. Furthermore, the rejection of Claims 5-7, 15-17 and 23-25 under 35 U.S.C. 103(a) as being unpatentable over Malek in view of Fish does not satisfy the requirements of a prima facie case of anticipation as claim limitations are not met by the cited references.

Accordingly, Applicants respectfully submit that the rejection of Claims 2-4 and 13 under 35 U.S.C. 112, second paragraph, the rejection of Claims 11-3, 8-14 and 18-22 under 35 U.S.C. 102(e), the rejection of Claims 1, 8 and 18 under U.S.C. 102(e) and that the rejection of Claims 5-7, 15-17 and 23-25 under 35 U.S.C. 103(a) are improper and should be reversed.

The Appellant wishes to encourage the Examiner or a member of the Board of Patent Appeals to telephone the Appellant's undersigned representative if it is felt that a telephone conference could expedite prosecution.

Respectfully submitted,

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Claims Appendix

1. (original) A computer implemented method for establishing a run-time data area comprising:

relocating a firmware module from a read-only memory location to a writeable memory location during a system boot-up operation;

reserving a portion of said writeable memory location comprising a memory allocation for said firmware module and an additional memory allocation; and

designating said additional memory allocation as said run-time data area, wherein said run-time data area is created without requiring prior knowledge of system resource allocation.

2. (original) The computer implemented method as recited in Claim 1 wherein said relocating further comprises:

receiving a system call for a system firmware feature; and

returning a response to said system call requesting said memory allocation for said firmware module, said additional memory allocation, and a memory allocation for said system firmware feature.

3. (original) The computer implemented method as recited in Claim 2 further comprising:

determining the size of said system firmware feature;

determining the size of said firmware module; and

determining the size of said run-time data area.

4. (original) The computer implemented method as recited in Claim 2 wherein said system firmware feature comprises a processor abstraction layer.

5. (original) The computer implemented method as recited in Claim 1 wherein said firmware module operates in a real mode.

6. (original) The computer implemented method as recited in Claim 1 wherein said firmware module operates in a virtual mode.

7. (original) The computer implemented method as recited in Claim 1 wherein said firmware module is dynamically operable in a real mode and a virtual mode.

8. (original) A method for creating a system independent run-time data storage area comprising:

intercepting a system call for determining the size of a system firmware feature during a system boot-up operation;

returning a response to said system call conveying a request for a portion of a writeable memory location; and

reserving a portion of said writeable memory location, wherein a memory allocation is designated as said run-time data area, wherein said run-time data area is created without requiring prior knowledge of system resource allocation.

9. (original) The method as recited in Claim 8 further comprising:

utilizing a firmware module resident upon a read-only memory location to perform said intercepting.

10. (original) The method as recited in Claim 9 further comprising:

relocating said system firmware feature and said firmware module from said read-only memory location to said writeable memory location.

11. (original) The method as recited in Claim 10 wherein said run-time data area comprises a sub-component of said firmware module.

12. (original) The method as recited in Claim 10 wherein said run-time data area is separate from said firmware module and said system firmware feature.

13. (previously presented) The method as recited in Claim 8 wherein said system boot-up operation is performed by a processor.

14. (original) The method as recited in Claim 13 wherein said system firmware feature comprises a processor abstraction layer.

15. (original) The as recited in Claim 9 wherein said firmware module operates in a real mode.

16. (original) The method as recited in Claim 9 wherein said firmware module operates in a virtual mode.

17. (original) The method as recited in Claim 9 wherein said firmware module is dynamically operable in a real mode and a virtual mode.

18. (original) A method for creating a run-time data area comprising:

receiving a system call for relocating a system firmware feature from a read-only memory location to a writeable memory location during a system boot-up operation;

allocating a first portion of said writeable memory location for said system firmware feature; and

allocating an additional portion of said writeable memory location and designating said additional memory allocation as said run-time data area, wherein said run-time data area is created without requiring prior knowledge of system resource allocation.

19. (original) The method as recited in Claim 18 wherein said system firmware feature comprises a processor abstraction layer.

20. (previously presented) The method as recited in Claim 18 further comprising:

using a firmware module to perform said receiving.

21. (original) The method as recited in Claim 20 further comprising:

allocating a third portion of said writeable memory location to said firmware module.

22. (original) The method as recited in Claim 20 further comprising:

allocating said additional portion of said writeable memory location to said firmware module; and

designating a portion of said firmware module as said run-time data area.

23. (original) The method as recited in Claim 20 wherein said firmware module operates in a real mode.

24. (original) The computer implemented method as recited in Claim 20 wherein said firmware module operates in a virtual mode.

25. (original) The computer implemented method as recited in Claim 20 wherein said firmware module is dynamically operable in a real mode and a virtual mode.

Evidence Appendix

None

Related Proceedings Appendix

None